UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/404,923	09/24/1999	FRANCOIS DOUEZY	02282.P034	8917

25943 7590 10/23/2002

SCHWABE, WILLIAMSON & WYATT, P.C.
10260 SW GREENBURG ROAD
SUITE 820
PORTLAND, OR 97223

EXAMINER
MAKHDOOM, SAMARINA

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/404,923	Applicant(s) DOUEZY ET AL
	Examiner Samarina Makhdoom	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The formal drawings were received on February 23, 2000. These drawings are approved by the draftsman and accepted by the Examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krakirian, U.S. Patent No. 6,064,247 in view of Trimberger, U.S. Patent No. 5,701,441.

As per Claims 1 and 8, Krakirian discloses a method for clock generation and distribution in an emulation system comprising:

generating a derived clock signal from a look up table, wherein an index to the

look up table is generated by counting cycles of a base clock signal (See Col. 4, lines 39 et Seq and Table I. The clock output and input signals are presented in Table 1 to provide a glitch-free clock. Also See Col. 2, lines 25 et Seq for the use of a counter to divide down the frequency of the input (i.e. base) clock signal for the output (derived) clock signal. Therefore the lookup table contains the binary values needed to generate the output (derived) clock signals);

Krakirian does not explicitly teach emulating the clock generating circuit, stopping the emulation, or restarting the emulation.

Trimberger discloses emulating a Field Programmable Gate Array with multiple sequencers, each sequencer allows operation with multiple user clocks. (See Col. 17, lines 21 et Seq) therefore teaching the emulation of a clock signal. Trimberger also discloses emulating an internal or external signal indicate a stop condition (See Col. 17, lines 44-56) therefore stopping the emulation. Trimberger also discloses running a sub-network that may be pre-empted (or stopped) and placed in a waiting state for resources to become available. Once the resources are available the running or emulating the sub-network is restarted (See Col. 37, lines 13 et Seq) therefore Trimberger teaches restarting the emulation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multiple frequency clock generation circuit of Krakirian with the emulation of Trimberger because it would allow Krakirian to emulate the clock generation circuit and evaluate it's performance before manufacturing the circuit saving both time and money.

As per Claims 2 and 9, Krakirian discloses the step of generating a derived clock further comprises:

accessing an entry in a look up table having an address corresponding to the number of intermediate clock signals that have been counted (See Col. 2, lines 25 et Seq for the use of a counter. This counter can be used for counting signals in a look up table like an index marker);

and outputting a signal level in response to the entry accessed (See Col. 4, lines 13 et Seq and Table 1. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN).

As per Claim 3, Krakirian a clock generation circuit comprising:

a base clock generation circuit that generates a base clock signal of a first frequency, and a derived clock generation circuit having (See Col. 3, lines 45 et Seq. for the disclosure of a clock generation circuit having an apparatus to generate multiple frequency output (derived) clock signals from an input (base) clock signal),

a frequency divider circuit coupled to receive the base clock signal (See Figure 6A for a Frequency Control Module item 600. Col. 6, lines 20 et Seq. disclose that the frequency control module 600 generates multiple frequency output clock signals that are twice, three, and four times the duration of the input (base) clock signal. Therefore the clock signal frequency is divided into half, thirds, or fourths),

a counter circuit coupled to receive an output of the frequency divider circuit (See Col. 2, lines 25 et Seq for the use of a counter to divide down the frequency of the input (i.e. base) clock signal for the output (derived) clock signal), and

a look up table coupled to receive an output of the counter circuit (See Col. 4, lines 13 et Seq and Table 1 – a truth or look up table. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN),

wherein the output of the counter circuit is used to index entries in the look up table (See Col. 4, lines 13 et Seq and Table 1 – a truth or look up table. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN),

and further wherein the entries in the look up table indicate a signal level for a derived clock signal generated by the clock generation circuitry (See Col. 4, lines 13 et Seq and Table 1. Table 1 contains the input clock signal CIN, is gated with two control signals CnH and CnL. The output (derived) clock signal is Cn, where n is an integer multiple of the input (base) clock signal CIN thereby indicating a signal level for the derived clock signal).

As per Claim 4, Krakirian discloses a plurality of clock generation circuits coupled in parallel to generate a plurality of derived clock signals (See Figure 6A, for the generation of clock signals in parallel and the corresponding text in Col. 6, lines 13 et Seq).

As per claims 5 -7 Krakirian does not teach emulating the clock generating circuit or the use of a multiplexor.

Trimberger discloses emulating a Field Programmable Gate Array with multiple sequencers, each sequencer allows operation with multiple user clocks. (See Col. 17,

lines 21 et Seq) therefore Trimberger emulates clock signals. Trimberger also discloses micro cycle sequencing in a time-multiplexed programmable logic device. In order to time multiplex signals, a multiplexor circuit is inherent (See Col. 25, lines 60 et Seq) therefore, the reference teaches the use of a multiplexor to time multiplex signals.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multiple frequency clock generation circuit of Krakirian with the emulation of Trimberger because it would allow Krakirian to emulate the clock generation circuit before manufacturing the circuit saving both time and money.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Beatty et al. U.S. Patent No. 6,055,489, disclose an integrated circuit including a comparator, a look-up table, and a timer circuit.

Kawasaki et al. U.S. Patent No. 5,838,956, disclose a clock generating circuit which generates a clock signal at a desired frequency.

Mirov et al. U.S. Patent No. 5,491,442, disclose a clock generator that produces a plurality of clock signals from a master clock.

Eun U.S. Patent No. 5,954,787, disclose a method of generating sin/cosine functions and apparatus using the same digital signal processor.

Sutherland, U.S. Patent No. 6,304,125, disclose a method of generating and distributing clock signals.

Decker et al. U.S. Patent No. 4,759,014, disclose digital data received on a plurality of input channels at unrelated, asynchronous input clock rates.

Lee et al. U.S. Patent No. 6,392,496, disclose a digital processing PLL circuit for comparing a first clock signal input and a second clock signal from feedback.

Stefek et al. U.S. Patent No. 6,135,648 disclose a hard disk simulator with a timing generator controller.

Rahkonen, T.; Eksyma, H., "A 3-V programmable clock generator with a built-in phase interpolator," Proceedings of the 1998 Midwest Symposium on Circuits and Systems, 1998. Pages: 488 –491.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samarina Makhdoom whose telephone number is 703-305-7209. The examiner can normally be reached on Full Time on Tuesday, Thursday, Friday, and Sunday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J. Teska can be reached on 703-305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0040 for regular communications and 703-305-0040 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

SM
October 18, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER